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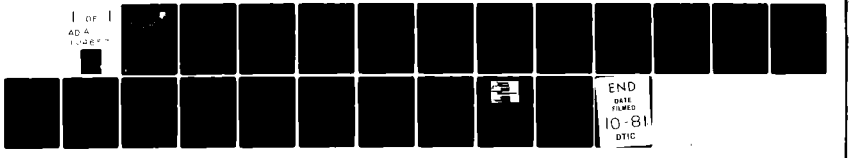

RADC-TR-81-66
Final Technical Report
June 1981

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R&D SERVICES TO DEVELOP AN IMPROVED ISOLATION TECHNOLOGY FOR RADIATION HARDENED BIPOLAR INTEGRATED CIRCUITS (PEDIC)

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes work performed in the development of a dielectrically isolated integrated circuit process for fabricating radiation hardened integrated circuits. The improved process, called PEDIC (Post Epitaxial Dielectrically Isolated Circuits), provides advantages over standard DI processes: radiation tolerant improvements, lower cost, faster turnaround time, better electrical performance, and greater packing density. Electrical test data from a 2-input NAND gate circuit

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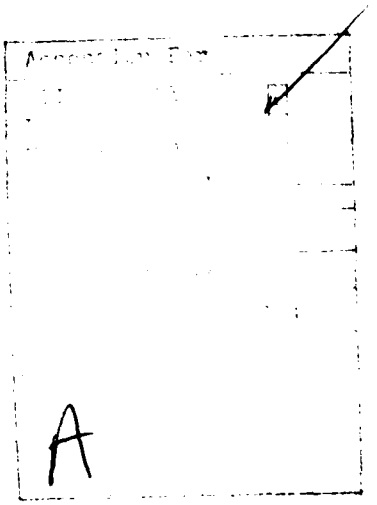
fabricated in the PEDIC structure is also given.

PREFACE

This report was prepared by the Military Products department of Texas Instruments Incorporated, Dallas, Texas, under Air Force Contract No. F19628-78-C-0205. The contract was monitored under the technical direction of Walter M. Shedd, RADC/ESR, Electronic Systems Division, Air Force Systems Command, USAF, Hanscom AFB, Massachusetts.

R&D Status Report Nos. 1 through 7 cover work performed under this contract from August 1978 to May 1980.

Key Texas Instruments personnel are Mr. Curtis Randolph, Program Manager; Mr Edward Jeffrey, Radiation Hardened Circuit Design Manager; and Mr. C. C. Shen, Device Processing. Silicon Materials department (SMD) key personnel in the material improvement phase are Mr. Lee Jones, Advanced Products Engineering Program Manager; Dr. John Robinson, Manager Development Engineering; and Mr. Mike Miller, Product Engineer.



SUMMARY

In the production of the 2-inch diameter PEDIC material, there were no obstacles encountered that were beyond the control of current processing procedures. At the first polish step, the anticipated dish was present, but its magnitude did not preclude the required level of single crystal thickness control. Slice bow decreased that control, but the amount of bow encountered on 2-inch material falls within routine process capabilities.

Forty-six PEDIC wafers were used to fabricate the quad 2-input NAND gate (MPD11269), which verified that the process has production capability. Twenty fully tested devices were delivered in addition to 25 basic PEDIC wafers.

A comparison of the modified PEDIC process with the standard single and double poly processes is shown in Table 1. The advantage of epi thickness control and surface quality of the PEDIC process over the standard single poly process allows a much improved radiation tolerant process to be used to fabricate integrated circuits. A 2X improvement in gamma dot threshold is estimated, as well as a 10X improvement in neutron tolerance if a shallow base ion implanted transistor process were used.

In order to realize the maximum gain from applying the PEDIC process for improved single crystal thickness control in DI material, the process must be extended to 3-inch material. The greater degree of bow and nonuniform deposition across the larger slice will require additional development, but the increased control to peripheral surface of the larger diameter would justify the effort.

Table 1. Die Process Comparison

Factor	Single Poly	Double Poly	Modified PEDIC
(nn^+) Layer Thickness	±0.15 mil	±0.2 mil	±0.15 mil
Surface to n^+ Thickness	±0.2 mil	±0.05 mil	±0.02 mil
Slice Bow	±1.5 mils	(2-3) mils	±2 mils
Usable Area	70 %	50 %	80 %
Up-Diffusion	Uncontrolled	Significant	Insignificant
Surface Quality (Min. Junction Depth)	1.4 μm	0.25 μm	0.25 μm
Material Lead Time	1X	1.5X	0.8X
Material Cost	1X	2.5X	1.5X
Final Bar Cost	1X	2.4X	0.6X
Useful Circuit Designs	80 %	100 %	100 %

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SECTION I
INTRODUCTION

The objective of this program is to develop a dielectrically isolated integrated circuit process suitable for the fabrication of radiation hardened integrated circuits. The process provides a substrate consisting of layers of n silicon (collector) on n^+ silicon (buried collector) on silicon dioxide (insulator) on polysilicon (mechanical support). These layers require thickness and resistivities appropriate for the fabrication of bipolar digital integrated circuits. In addition, the process yields a substrate (wafer) which is not dependent on the particular integrated circuit to be fabricated. Final isolation occurs at the start of specific circuit processing.

This program investigates and compares present bipolar dielectrically isolated processes. This comparison considers the uniformity of device pocket depth and resistivity across the wafer, the degree of wafer bowing, usable wafer area for device processing, and surface quality of the wafer.

As a result of this investigation, an improved process for the fabrication of dielectrically isolated substrates that offers improvements in control for collector depth and out-diffusion of the buried layer has been defined. The usable area of the wafer is an improvement over present processes. The level at which it is economically feasible to standardize the DI wafer is determined, and the possibility of extending the bipolar DI technology to large-scale integration is evaluated.

The improved dielectric isolation process is evaluated for improvement in the nuclear radiation hardness of circuits fabricated in the substrate. Tolerance to neutron radiation and upset caused by transient ionizing radiation is considered.

Test lots of dielectrically isolated substrates verify the process that can be used for the subsequent production of integrated circuits.

The quad 2-input NAND gate integrated circuit is used as a test vehicle, and is fabricated in the dielectrically isolated substrate to demonstrate that ICs can be built in these substrates.

SECTION II
TECHNICAL DISCUSSION

A. PRESENT DI PROCESSES

DI processes may be divided into two methods: (1) precision grind, lap, and polish, and (2) double poly. Each method has its own advantages and disadvantages as related to device performance and to problems of substrate fabrication. The materials have been primarily [100] and [111] orientation Si, with early work using [111] because of its common use at that time. Current work uses primarily [100]. The preference for [100] is due to a combination of the fourfold symmetry of the [100] system and the fast orientation-dependent (OD) etching in the [100] direction, which provides built-in process control.

1. Single Poly Process

The precision grind, lap, and polish process (sometimes referred to as single poly) with an n^+ buried layer to reduce collector saturation resistance is shown in Figure 1. An oxide is grown on the substrate, whose resistivity is determined by the desired collector resistivity, and windows opened by conventional photolithography. These windows allow the isolation moats to be etched, usually with an orientation-dependent etch that attacks the silicon in the [100] direction as much as 100 times faster than in the [111] direction. Thus, the cross section of an etched groove will appear triangular, as shown in Figure 1, if the mask is aligned on the slice so that the grooves are parallel with the traces of the [100] system in silicon. Adjacent sides of a rectangular mask can be aligned with the traces of [111] planes on the [100] surface so that square or rectangular arrays of grooves can be etched. Due to the large difference in etch rate in the [100] versus [111] directions, when the etch reaches the [111] plane intersecting the [100] surface at the edge of the mask, the etch rate becomes less than 0.03 μm/min and for practical purposes, etching stops.* Since the [111] planes intersect the [100] surface at a fixed angle (54.74 degrees), the width of the oxide opening determines the depth of the OD (isolation) etch moat. After the isolation moats are etched, an n^+ diffusion or a heavily doped epitaxial film may be deposited across the entire surface. A thermal oxide is then grown across the top of the wafer. This oxide becomes the isolation between the single crystal and a polycrystalline silicon layer that is added next. The thickness of this layer is approximately equal to the thickness of the original slice, in general 15 to 20 mils. The polycrystalline silicon deposition can be made in a conventional epitaxial reactor using a silicon halide-hydrogen reduction process. For example, 10-mole-percent (m-%) $SiHCl_3$ in hydrogen at 1150°C gives a deposition rate of about 10 μm of polycrystalline silicon per minute. After the polycrystalline silicon is deposited, the poly surface is ground on a Blanchard or similar type surface grinder to re-establish parallelism between the top of the slice (polycrystalline silicon) and the bottom (original

*The effective mask undercutting and the measured etch rate at this point are a strong function of how carefully the mask is aligned to <111> traces.

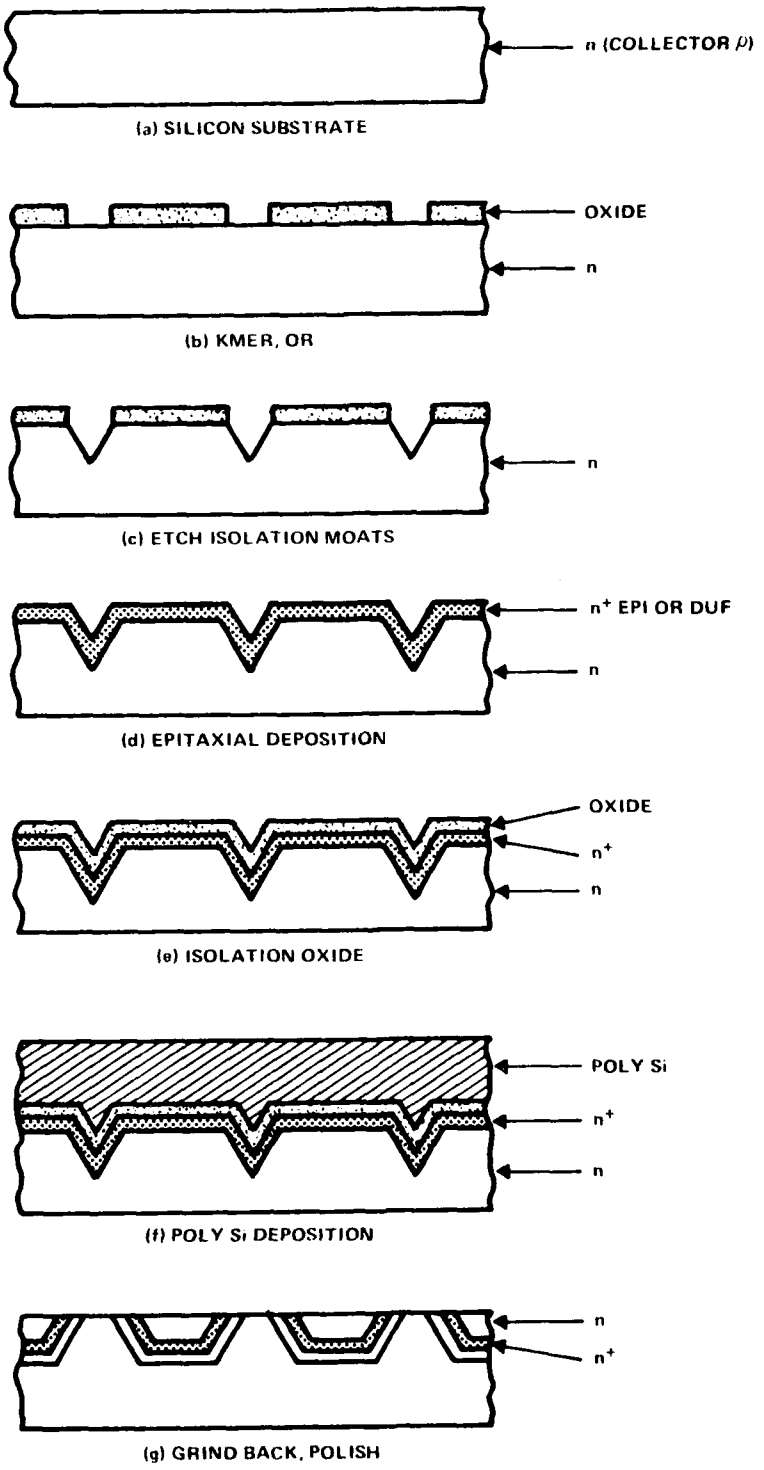


Figure 1. Standardized DI Process
(Precision grind, lap and polish method, and surface n^+ contact)

single crystal silicon substrate) of the slice. Should deposition conditions be such that a polycrystalline lip is present on the single crystal side, the lip must first be removed to allow the slice to seat well on the grinder chuck. The slice is then inverted and the original substrate is ground back far enough to reveal the isolation oxide in the deepest thickness indicators (which may be the scribe lines) and the single crystal islands of silicon, and then polished. After polish, the slice is ready for conventional device processing except that the isolation diffusion steps are eliminated. In the process described, an n^+ surface collector contact is provided by the epi or diffused n^+ film. If a buried layer of n^+ material is desired that does not contact the top surface, the epi or diffusion may be performed prior to step (b) in the process. In that case, the isolation moats are etched through the buried layer, thus leaving it across the bottom of the final isolated tank. The precision grind and polish process is fairly simple compared to other processes but the final surface is mechanically polished and the uniformity of the n-layer thickness across the slice is determined by how nearly parallel the final surface is (after lap and polish) with the original one.

2. Double Poly Process

Figure 2 shows the somewhat more complicated double poly process. To understand this process, skip to step (d) in the figure and neglect for the moment the grind indicators mentioned in steps (b) and (c). An n-epi film, the thickness and resistivity determined by the collector parameters of the device or circuit to be fabricated, is deposited over the n^+ substrate. An SiO_2 layer called the separation oxide is grown or reactor deposited across the epi surface. Next, a temporary polycrystalline silicon layer is grown over the oxide. The slice is inverted and ground and polished back to a thickness equal to that of the epi layer plus a suitable amount of n^+. At this point a problem arises. Unless great care is taken in keeping track of reference surfaces and the amount of material removed, there is no way of knowing when to stop lapping. To assist in this, the thickness indicator grooves shown in steps (b) and (c) of Figure 2 are used * When the grinder or polisher cuts through to these grooves and they become visible, the operator can stop grinding or polishing. There will normally be a series of grooves of increasing depth to assist in more accurate control. Assuming no mask undercutting, the depth (d) of an indicator groove is given by

$$d = (W/2) \tan \theta$$

where W is the width of the mask opening and θ is the angle the appropriate {111} plane makes with the surface {54.7 degrees for a (100) surface}. Typically, six to eight depths will be used in an array, and the array will be placed in five positions over the slice for double poly process or in each circuit bar for single poly processing.

Oxide is thermally grown or deposited across the surface. The oxide is opened for isolation moats as in the single poly process. However, in this case, the moat depth will not be determined by the oxide opening, but by the distance to the separation oxide. An isolation oxide is then thermally grown or vapor deposited. A second polysilicon deposition is made over the isolation oxide. The slice is then inverted and the first poly silicon layer is ground, polished, and/or chemically etched back to the original epi film surface which is protected by the separation oxide. As can be seen in

*The same problem also occurs in single poly and thickness indicators are used.

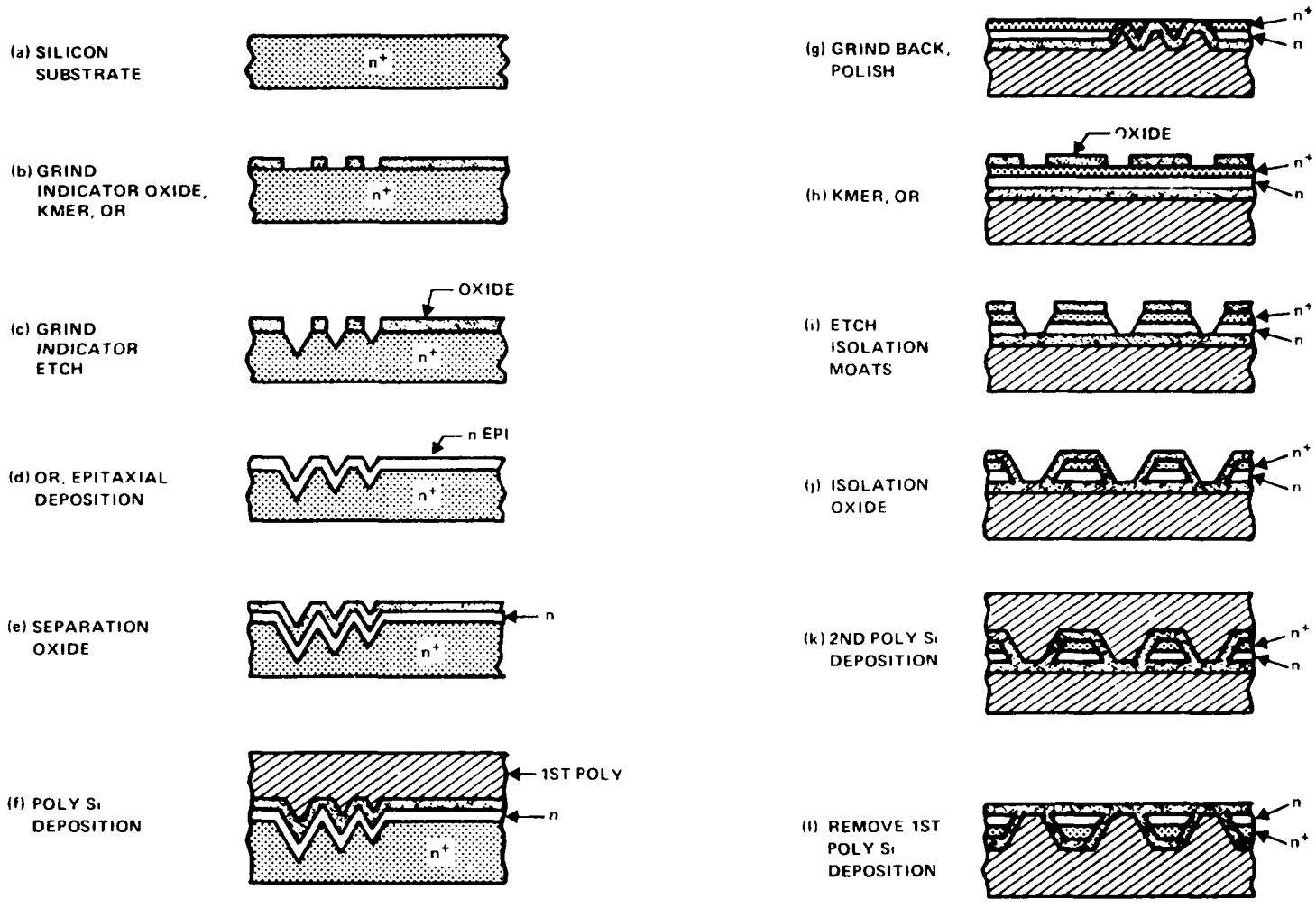


Figure 2. Double Polycrystalline Silicon DI Process

Figure 2, the resulting structure is a dielectrically isolated epitaxial film above an n^+ buried layer. This process is used in cases where very exact control of the collector thickness is required. It is long and costly but provides a good surface for the fabrication of shallow devices since they are formed in an epitaxial film that has not been subjected to mechanical or wet chemical processing.

B. STATEMENT OF PROBLEM

Dielectric isolation has been utilized for over a decade to provide electrical isolation between components during radiation exposure. The single poly DI structure is presently utilized for over 90 percent of all DI designs, and has moved quite far down the learning curve. However, there are several problems inherent with the single poly process itself. First, there is the question of pocket thickness control specifically, control of the n layer thickness to the n^+ buried layer. Second, the surface quality on chemical-mechanical polished surfaces is poor even with an additional HCl chemical etch. Third, the turnaround time is excessively long for new DI mask changes.

The first problem was solved by double poly material to some extent since an epi layer of well controlled thickness is utilized. However, the overall surface to n^+ distance may vary considerably because of n^+ up-diffusion during the second high-temperature polysilicon deposition. Better control is required on both the n layer and the total nn^+ pocket thickness for switching characteristics as well as radiation response.

The second problem was partially solved by using a chemical etch prior to first oxidation followed by a stress relief process consisting of a first oxidation; a high-temperature anneal which activates deep dislocations; a stress relief OR which gives dislocation pin sites; and a second oxidation which mobilizes the surface defects so that they migrate to the corners of the stress relief pattern where they are pinned away from active junctions. The surface quality is adequate for many applications, but MSI devices with junctions of less than 1.4 μm in depth run low yields. However, double poly solved this problem with a polish-free surface, which allows 0.25-μm junction devices to be readily fabricated.

The third problem is inherent to the early dedication of a DI isolation mask to a given substrate. The double poly material is even worse.

The effort described by this program to solve the preceding problems demonstrates the post-epitaxial dielectrically isolated circuit (PEDIC), first described by Motorola, which has been modified to meet broader wafer processing constraints which will be required for wider usage by various semiconductor vendors.

C. THE POST-EPITAXIAL DIELECTRICALLY ISOLATED CIRCUIT PROCESS

The PEDIC structure begins with a Czochralski grown ⟨100⟩ (±0.5 degree) antimony substrate with an n-type resistivity of 0.008 to 0.020 ohm-cm. Thickness is controlled to 21 ±1 mil. The most critical substrate parameters are bow and taper; these are controlled within 0.3 mil.

Initial oxidation, as shown in Figure 3(a) is accomplished in a Thermco Brute American XL furnace. The oxidation ambient is steam at 1100°C to a thickness of 10,000 ±500Å. Oxide thickness monitoring is accomplished using a Nanometrics Microarea Film Thickness Gauge. Fine control of the initial oxidation thickness will minimize errors in depth indicator width variations due to oxide

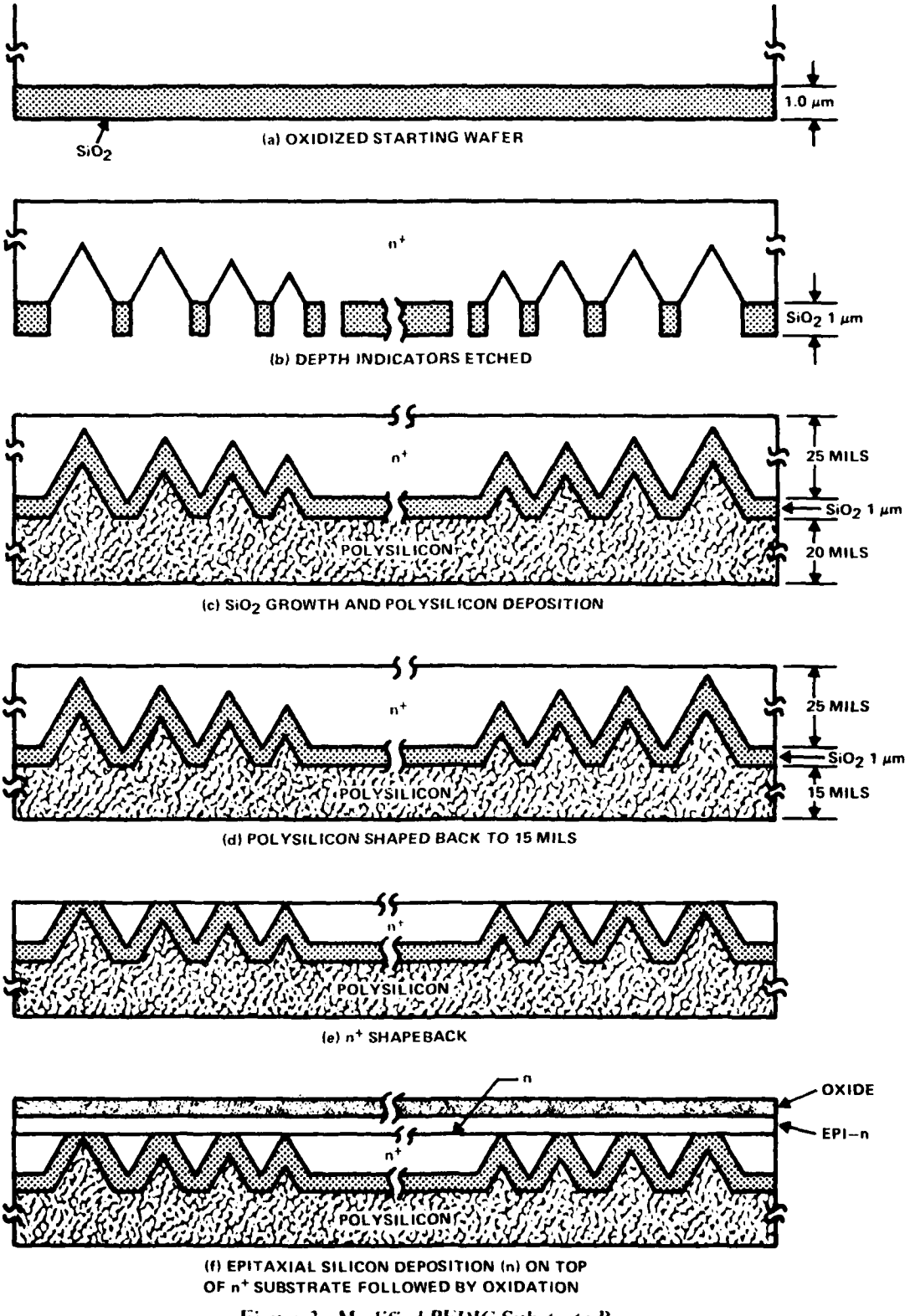


Figure 3. Modified PEDIC Substrate Process

thickness variations, with a resultant finer control of the final OD etched depths. Oxide patterning is done using conventional photolithographic and oxide etching techniques in a Class 100 VLF cleanroom environment. Depth indicators are defined as in Figure 3(b), using a potassium hydroxide selective OD etch with resulting V-channels bounded by (111) planes. Channel reference depths of 0.6 ±0.1 mil is targeted in five locations on each substrate (Figure 4).

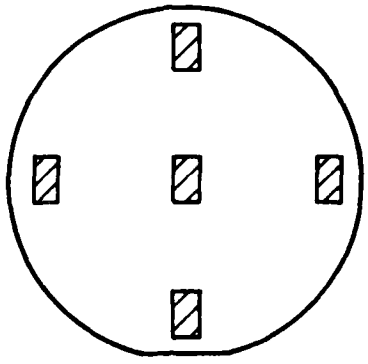


Figure 4. Depth Indicator Location on Wafer

Subsequent to the depth indicator definition, a uniform isolation oxide is grown over the complete substrate, using the previously discussed oxidation conditions. This isolation oxidation is followed by a 1200°C perchloroethylene gettering process to remove oxidation-induced stacking faults and dislocation loops. This procedure minimizes device leakage currents associated with oxidation induced material defects.

The initial polysilicon deposition is made, as shown in Figure 3(c), to a controlled thickness of 20 ±2 mils. Substrate warpage is reduced by thermally cycling the polysilicon reactor with optimized time rates of temperature change.

The polysilicon final thickness definition is done using standard planar grinding techniques. The n^+ layer thickness is defined using an identical planar grinding procedure coupled with precision lapping and polishing. The single array Strasbaugh polishing technique, developed under the AFML contract (to improve standard DI) is applied to achieve ±0.1-mil control of the n^+ layer thickness, as shown in Figure 3(e).

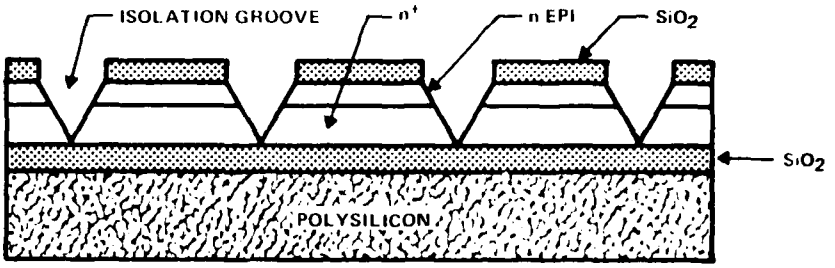
Any residual damage from the chemical-mechanical polishing is removed during the epitaxial deposition process by a predeposition HCl vapor etch. The epitaxy process is done using a dichlorosilane process in an Applied Materials Model 7000 epitaxy reactor. Reactor temperature is 1090° ±5°C, and the reactor design assumes a slip-free epitaxial layer. The epitaxial film is 6.3 ±0.4 μm thick and 0.3 ±0.03 ohm-cm resistivity. The oxidation for storage and/or final device patterning is 1.0 ±0.05 μm thick, and processed identically to the previous oxidation steps, as is shown in Figure 3(f).

The result of material processing to this point is a finely controlled silicon n on n^+ substrate, which controls not only the thickness of the epitaxial layer, but the total nn^+ tub depth. The tightly controlled n layer allows for better control of device electrical parameters and a well established value for R_{CS}. The tight control on the n^+ layer thickness improves the total control of collector resistance and on photocurrent generation volumes. The combination results in a significant improvement in both design capability and radiation hardness repeatability. In addition, the epitaxy surface has not been mechanically damaged by polishing, and should, therefore, be comparable to double poly surfaces, which allow the fabrication of ultrashallow ion implanted transistor structures ($\leqslant 0.4$ μm deep bases) which have demonstrated orders of magnitude increases in radiation tolerance.

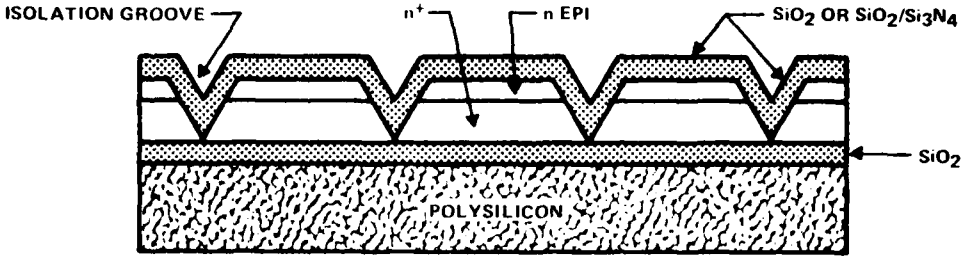
Up to this point in materials processing, the substrate is independent of the DI or bar layout design since no device patterns have been incorporated into the structure. This allows for a ready supply of epitaxial substrates for DI applications which cuts off 60 percent of the required materials fabrication time before commitment to a specific device design geometry is required. This allows for quicker turnaround on new designs as well as a lower substrate cost once a number of critical epitaxial resistivity/thickness ranges have been established for volume production. The processing at this point is also sufficient for larger substrate fabrication (3-inch DI, 100 mm, etc.) at better yield capability than presently available.

Final device and circuit definition is initiated by patterning the isolation level and selectively etching the nn^+ material, Figure 5(a), using a potassium hydroxide OD etchant as previously described. If a wraparound n^+ collector should be required, a short deposition cycle could be added at this point. The MX design utilized in this activity does not require such an exotic process. When the single crystal islands have been etched, the DI process may be finalized by applying either a composite SiO_2/Si_3N_4 passivation scheme or an SiO_2 passivation layer. Each has its device fabrication process flow requirements. The SiO_2 layer was selected for this activity, because the later processing sequences had demonstrated that thermal stress induced cracking of Si_3N_4 layers caused by the "parrot's beak" effect. Other wafer fabrication process flows, such as the all-implanted transistor process flows, could utilize the SiO_2/Si_3N_4 structure to great advantage. Figure 5(b) shows the modified PFDIC structure with a dielectric layer providing the sidewall isolation. The SiO_2 layer is 1.0 ± 0.05 μm whereas the SiO_2/Si_3N_4 composite would require 0.12 ± 0.02 μm thickness achieved through the reaction of ammonia with dichlorosilane. The nitride layer properties are 1.92 to 2.05 index of refraction with an etch rate of 7 to 13 Å/min in 32°C buffered HF.

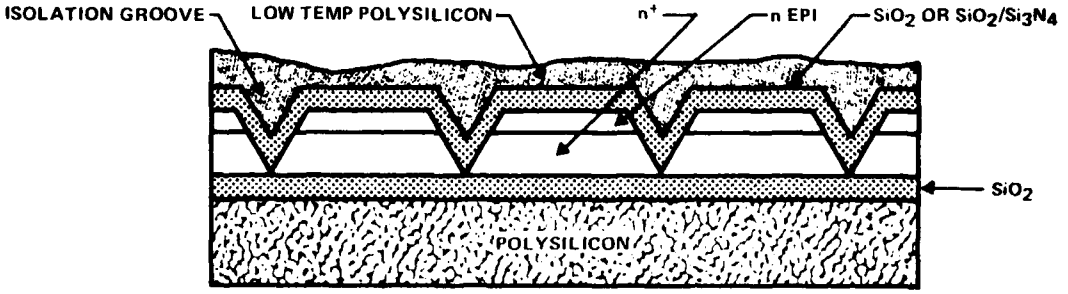
The final steps before device fabrication are polysilicon fill and shape back. The polysilicon fill process, as shown in Figure 5(c), is a low-temperature process which minimizes slice warpage and n^+, up-diffusion. Deposition rates of 0.54 μm/min are achievable at 900°C. The total reaction time is approximately 50 min. The precision grinding and polishing advances attained under the AFML contract are utilized for the final polysilicon shape back. Figure 5(d) shows the final PFDIC structure before device fabrication.



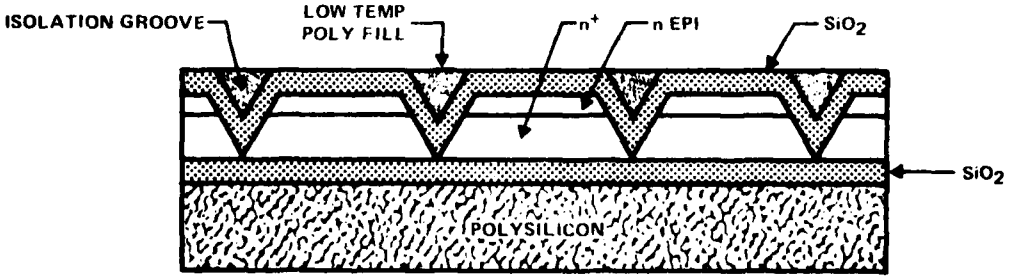
(a) OD ETCHED TUBS (nn^+)



(b) DIELECTRIC ISOLATION SiO_2 OR SiO_2/S_3N_4



(c) LOW TEMPERATURE POLYSILICON DEPOSITION



(d) FINAL STRUCTURE READY FOR DEVICE FABRICATION

Figure 5. Modified PEDIC DI Process

D. TEST CIRCUIT FABRICATION

The MPD11269, a quad 2-input NAND gate integrated circuit (Figure 6) developed for the MX AGS program, was used as a test vehicle to demonstrate fabrication feasibility on the modified PEDIC substrate. The process is low power Schottky and identical to the standard flow used on the single poly version. The process flow is shown in Figure 7. No changes were made to the photomask tooling except for the isolation due to the front side isolation requirement of the PEDIC process.

Eleven PEDIC wafers were processed out of the front end and into multiprobe. Both ac and dc testing were performed at 25°C and 125°C. The overall yield was 5.2%. A major yield loss occurred due to etched channels along the isolation oxide. This occurred because single poly isolation design tolerance (isolation to stress relief O.R. separation) was not compatible with the front side PEDIC isolation. A normally allowable misalignment caused the stress relief O.R. definition to be exposed along the isolation oxide. At oxide removal, the isolation oxide was etched below the surface, causing a channel effect (see Figure 8). This is easily rectified by allowing more separation between isolation and O.R. definitions.

A test summary of the PEDIC structured 2-input NAND gate circuit with comparison data to standard DI is shown in Table 2. Evaluation of the processed PEDIC lot indicated transistor gain (H_{FE}) was on the low side. The minimum transistor gain process goal is 60. Transistor gains for the PEDIC lot were around 40.

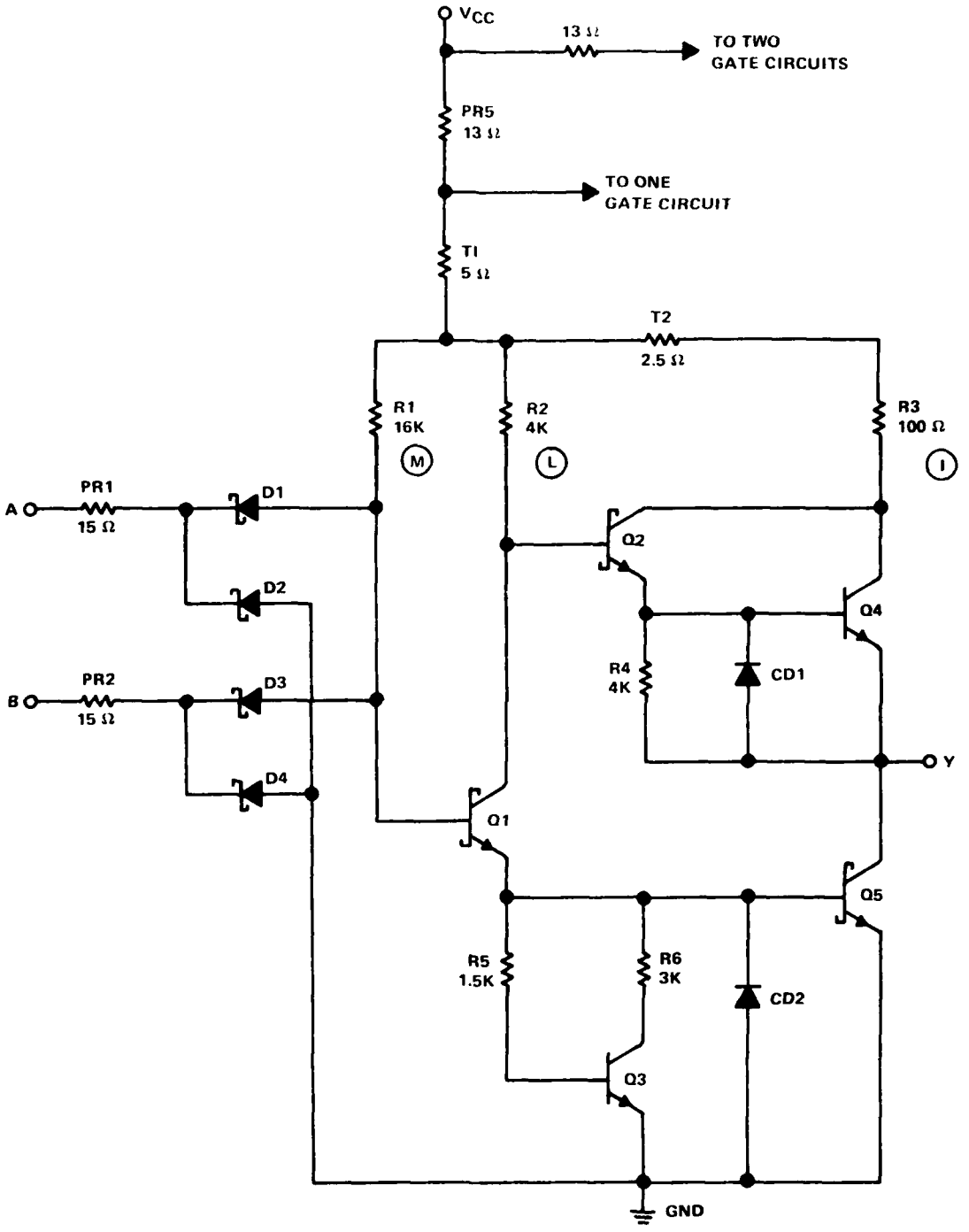


Figure 6. PEDIC Test Circuit Schematic

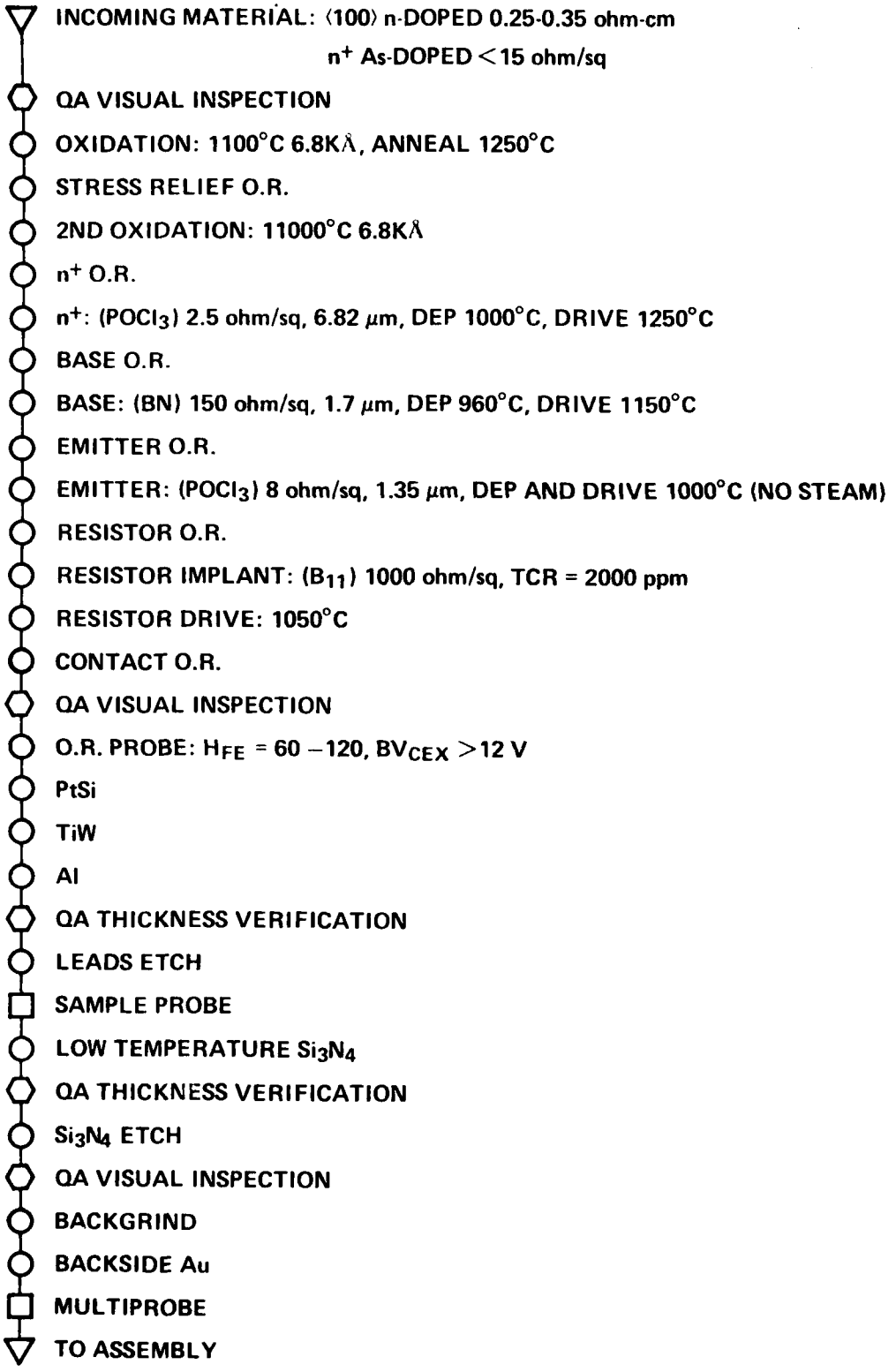


Figure 7. Process Flow (MPD11269)

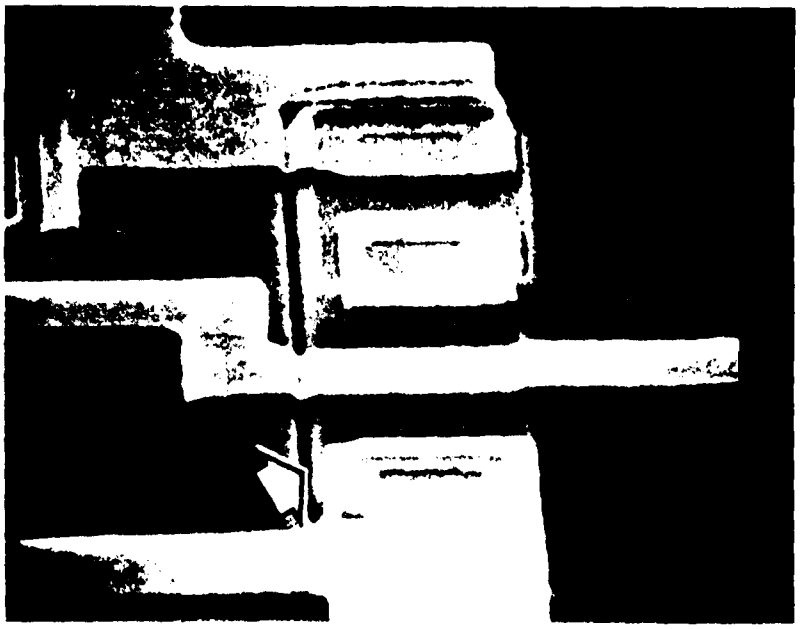


Figure 8. Etched Channel in Isolation Oxide

Table 2. Test Summary of 2-Input NAND Gate (MPD11269)
PEDIC Structured Vs Standard DI

Parameters		25°C		125°C		Units
		X	Std. Dev.	X	Std. Dev.	
V_{OH}	PEDIC	2.97	0.007	2.95	0.03	V
	S.D.I.	3.03	0.04	2.94	0.10	V
V_{OL}	PEDIC	0.235	0.005	0.209	0.004	V
	S.D.I.	0.230	0.006	0.207	0.008	V
V_{OLS}	PEDIC	0.149	0.002	0.109	0.007	V
	S.D.I.	0.157	0.004	0.117	0.006	V
V_{IC}	PEDIC	1.07	0.019	1.01	0.02	V
	S.D.I.	0.981	0.019	0.99	0.018	V
I_{IH}	PEDIC	0	0.03	0	0.8	µA
	S.D.I.	0	0.15	0	0.1	µA
I_{IL}	PEDIC	0.320	0.010	0.271	0.010	mA
	S.D.I.	0.271	0.013	0.219	0.011	mA
I_{OS}	PEDIC	32.3	0.9	30.8	0.75	mA
	S.D.I.	36.8	4.7	34.5	4.05	mA
ICCH	PEDIC	1.48	0.05	1.41	0.19	mA
	S.D.I.	1.15	0.118	0.936	0.111	mA
ICCL	PEDIC	6.43	0.18	5.87	0.17	mA
	S.D.I.	5.20	0.346	4.36	0.321	mA
T_{PDHL}	PEDIC	13.5	0.27	13.3	0.44	ns
	S.D.I.	11.3	0.69	12.8	0.73	ns
T_{PDLH}	PEDIC	7.55	0.12	8.9	0.13	ns
	S.D.I.	5.35	0.28	7.6	0.53	ns

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